Training Opportunity for Luxembourgish Trainees

Reference	Title	Duty Station
LU-2019-TEC-EDM	**Space Microelectronics**	**ESTEC**

Overview of the unit's mission:

The core responsibilities of the Microelectronics Section of the Data Systems and Microelectronics Division cover technical support to ESA missions and research activities in the areas of:

- digital and analogue integrated circuit [Application Specific Integrated Circuit (ASIC) and Field Programmable Gate Array (FPGA)] and Intellectual Property (IP) Core developments for space applications;
- mitigation techniques against radiation effects for ASICs and FPGAs;
- tools and methods for Integrated Circuit (IC) design and development (from specifications to tested devices).

The trainee will contribute substantially to one of the fields identified below, or a tailored set of objectives based on activities proposed below.

Overview of the field of activity proposed:

Within the field of space ASIC and FPGA microelectronics several different activities are proposed and described below:

1. Develop and test functional representative cases of Software Defined Hardware with the new European space FPGAs ("BRAVE")[1] implementing on-board data processing functions in collaboration with ESA colleagues. The work will include perform benchmarking of existing digital IP Cores relevant to the work, while also helping to identify areas of improvement in the programming tools in close collaboration with NanoXplore. The target FPGAs will be the BRAVE NG-LARGE and the NG-ULTRA FPGAs when available, the first worldwide radiation-hardened SoC-FPGA for space.

2. Investigate and evaluate the effectiveness of design mitigation techniques against radiation for the use in space applications of non rad-hard and Commercial-Off-The-Shelf (COTS) FPGAs. This activity is of major importance for the use of those FPGA in the "New Space". The target FPGA technologies include Xilinx Ultrascale and beyond, as well as Microsemi FPGAs.

3. Contribute to the implementation of a Reduced Instruction Set Computer-V (RISC-V) microprocessor test chip in advanced sub-micron ASIC technology. This requires working with Integrated Circuit Computer-Aided Design (IC CAD) tools such as Mentor, Synopsys, Cadence.

4. Perform microelectronics design and/or test of analogue and mixed-signal new (IP Cores [2] and devices for space applications. ESA has several recently

developed and on-going devices and IP in Design Against Radiation Effects (DARE) 180nm [Single Event Transient (SET) test vehicle, Analogue to Digital Converter (ADC), Digital to Analogue Converter (DAC)], and would like to extend their electrical as radiation performance focusing in 65nm and lower technology nodes.

5. Simulation of the radiation effects on transistors and basic logic cells with 3D Technology Computer-Aided Design (TCAD) modelling tools for evaluation of technologies that we want to fly in space. ESA has already initiated research with Robust Chip tools for 180nm and 65nm technology of UMC, ST and TSMC. We would like to investigate other processes such as 28/22/12nm Fully Depleted Silicon-on-Insulator (FDSOI) and 14/12nm Fin Field Effect Transistor (FinFET).

6. Develop a demonstrator on a SystemC Virtual Platform [3], using such platform to solve an on-board data processing problem exploring different possible System-on-Chip (SoC) architectural solutions.

7. Investigate the High Level Synthesis design flow for space applications, including how to apply soft SEE mitigation techniques in such flow, targeting several FPGA devices such as BRAVE, Microsemi RTG4 or Xilinx Kintex Ultrascale.

[1] https://www.esa.int/Our_Activities/Space_Engineering_Technology/Shaping_the_Future/High_Density_European_Rad-Hard_SRAM-Based_FPGA-_First_Validated_Prototypes_BRAVE
[2] https://www.esa.int/Our_Activities/Space_Engineering_Technology/Microelectronics/Analogue_and_Mixed-Signal_IPs_for_Space
[3] https://www.esa.int/Our_Activities/Space_Engineering_Technology/Microelectronics/Virtual_Platform_Technology

Required education:

Applicants should have just completed (not more than three years ago) or be in their final year of a university course at Master's level in Microelectronics, with special interest in digital and/or analogue VLSI design and technology, and:

- Knowledge / experience with C, C++ and digital VHDL design tools (e.g. MENTOR, SYNOPSYS) or/and
- Knowledge / experience with analogue VLSI design tools (e.g. CADENCE, MENTOR) or/and
- Knowledge / experience with electrical tests of VLSI components

Knowledge / experience with radiation effects on semiconductors would be a valuable asset

Candidates must be fluent in written and spoken English